MiniTerm Associates, inc.

# ROM/EROM DOCUMENTATION

TABLE OF CONTENTS


| | Page |
|---|---|
| INTRODUCTION | 1 |
| PARTS LIST | 4 |
| ASSEMBLY | 5 |
| Assembly Diagram | 9 |
| JUMPER SELECTION | |
| Address Selection (1K Devices) | 10 |
| Address Selection (2K Devices) | 12 |
| Buffer Enable Select | 13 |
| RESTART JUMP | 14 |
| FRONT PANELLESS OPERATION | 15 |
| MEMORY DEVICE PERSONALITY JUMPERS | 16 |
| THEORY OF OPERATION | 18 |
| Schematic Diagram | 19 |
| SPECIAL CASES | 22 |


Copyright 1977 by MiniTerm Associates, inc.

FEATURES

* S-100 Bus compatible

* 8K storage with 2708 EROMS or 1K Mask ROMS (8308 or equivalent).

* 16K storage with 2716 EROMS or 2K Mask ROMS (8316E or equivalent).

* 12K storage with half 1K devices and half 2K devices.

* Two individually addressable memory blocks allows for optimum memory placemment.

* Restart Jump feature eliminates need for expensive front panels and system monitor boards. Does not require memory to have Phantom feature.

* DMA compatible memory and restart operation.

* Independent Enable - Each ROM device is individually enabled or disabled to the CPU bus. This allows other memory devices to be addressed within the same memory block and allows the ROM/EROM to use as little as 1K of memory space.

* All data and address lines are fully buffered.

* Memory Expansion Bank Select

* Optional Wait Logic

* Fully Socketted

* Front Panel Replacement MWrite Logic

* Card Ejectors

PARTS LIST
**********

| ITEM | QTY | PART NO. | DESIGNATION |
|---|---|---|---|
| 1 | 1 | PCB | PC - ROM/EROM |
| 2 | 1 | 74LS04 | A1 |
| 3 | 2 | 74LS20 | D1,G1 |
| 4 | 1 | 74LS30 | F1 |
| 5 | 1 | 74LS139 | D2 |
| 6 | 6 | 74LS367 | H1,K1,A2,B2,H2,K2 |
| 7 | 1 | 74LS02 | F2 |
| 8 | 1 | 74LS00 | G2 |
| 9 | 1 | 7905 -5V VR | VR1 |
| 10 | 1 | 7812 +12V VR | VR2 |
| 11 | 1 | 7805 +5V VR | VR3 |
| 12 | 5 | 3.3uF, 25V, 20% | C1,C3-C6 |
| 13 | 1 | 33uF, 10V, 20% | C2 |
| 14 | 23 | .05uF, 12V, 20% | C7-C30 |
| 15 | 9 | RC07 2K 5% | R1-R9 |
| 16 | 1 | RC07 470 ohm 5% | R10 |
| 17 | 6 | C8314-02 | 14 pin TI |
| 18 | 12 | C8316-02 | 16 pin TI |
| 19 | 8 | C8324-02 | 24 pin TI |
| 20 | 3 | 6-32x3/8 | RH screw |
| 21 | 3 | #6 KEP | KEP nut |
| 22 | 3 | 6016B-14 | Heat Sink, Thermalloy |
| 23 | 2 | S-205 | Card Ejectors, Scanbe |
| 24 | 2 | RP/S-205 | Roll Pins |
| 25 | 5 | ft 60/40 | Resin Core Solder |

## ASSEMBLY

Sockets are provided for all DIP integrated circuits and DIP jumper positions. All components are mounted on the component or top side of the board. Use only resin core solder as provided, and use a hot soldering iron with a small tip. Keep the iron tip clean by wiping frequently with a damp sponge or rag. Allow the solder to flow by keeping the iron tip to the solder joint for a fraction of a second after removing the unused solder. The solder should completely fill the hole around each lead and should be bright in appearance. Too much solder, as long as it doesn't cause solder bridges, is better than not enough. If a solder joint appears dull it may be a 'cold joint'. Reheat the joint while applying a little more solder. Adding more solder supplies more flux to aid the solder flow.

Follow the assembly procedure and check each component in the list as it is installed. The six tantalum capacitors must be inserted with correct polarization. When the board is completely soldered, it should be brushed with a small stiff brush to remove any solder splashes or lead clippings.

CAUTION: Do NOT install DIP ICs until the power supply regulators have been properly checked.

## RESISTORS

For each resistor listed below locate the resistor by color code and determine its position from the assembly diagram or the board silkscreen. Bend the leads to fit the PC board holes and insert the resistor from the component side of the board. Solder the leads on the reverse (solder side) of the board and clip the excess lead length. Be careful of your eyes. Save the clipped leads for later use as jumpers.

(✓) R1-R9 (Red-black-red) 2K 1/4 watt
(✓) R10 (Yellow-Violet-Brown) 470 ohm 1/4 watt

## IC SOCKETS

One of the following three methods should be used to install the IC sockets:

1. Install and solder each socket completely.

2. Install and solder only two corner pins of each socket to hold the socket in place for later mass soldering.

3. Install all sockets at once and use a piece of cardboard to hold them in place as the board is turned solder side up for soldering. If you use the last method it is best to solder two corner pins on each socket first and then check that all sockets are seated flat against the board. If any are not flat, simply press them to the board while heating the two corner pins on the solder side.

The IC sockets should be inserted such that the pin 1 indication (a small wedge) is on the lower side of the socket (towards the connector).

Solder eight twenty-four (24) pin sockets into the locations listed below:

| | | | | | |
|---|---|---|---|---|---|
| ( ) | 1. | A3 | ( ) | 5. | E3 |
| ( ) | 2. | B3 | ( ) | 6. | F3 |
| ( ) | 3. | C3 | ( ) | 7. | G3 |
| ( ) | 4. | D3 | ( ) | 8. | H3 |

Solder twelve sixteen (16) pin sockets in the locations listed below:

| | | | | | |
|---|---|---|---|---|---|
| ( ) | 1. | A2 | ( ) | 7. | E1 |
| ( ) | 2. | B1 | ( ) | 8. | E2 |
| ( ) | 3. | B2 | ( ) | 9. | H1 |
| ( ) | 4. | C1 | ( ) | 10. | H2 |
| ( ) | 5. | C2 | ( ) | 11. | K1 |
| ( ) | 6. | D2 | ( ) | 12. | K2 |

Solder six fourteen (14) pin sockets into the locations listed below:

| | | | | | |
|---|---|---|---|---|---|
| ( ) | 1. | A1 | ( ) | 4. | F2 |
| ( ) | 2. | D1 | ( ) | 5. | G1 |
| ( ) | 3. | F1 | ( ) | 6. | G2 |

## VOLTAGE REGULATORS

Three different voltage regulators are supplied with the ROM/EROM kit to provide the +12V, +5V and -5V required by the 2708 EROMs. Be sure to mount the regulators in their correct positions.

To mount a regulator and its heatsink, bend the leads of each regulator such that when they are inserted into the PC board, the mounting hole in the regulator tab lines up exactly with the corresponding hole in the PC board. Insert a #6 screw through the PC board from the SOLDER SIDE and place a heatsink over it from the component side. Insert the leads of the regulator into the PC board mounting holes and the tab over the screw shaft. The heatsink should be between the PC board and the regulator. Place a washer over the screw shaft and twist on a #6 nut and tighten.

Solder the regulator leads to the PC board and clip the excess lead length.

(✓) Install the 7905 (or LM320T-5) regulator and heatsink into position 1 nearest the edge connector.

(✓) Install the 7812 (or LM340T-12) regulator and heatsink into position 2 in the middle of the board.

(✓) Install the 7805 (or LM340T-5) regulator and heatsink into position 3 nearest the top of the board.

## CAPACITORS

Tantalum capacitors are polarized and MUST BE INSTALLED WITH CORRECT POLARIZATION. The positive mounting lead position is indicated on the PC boards by a plus "+" sign in foil. A small dot, plus sign or vertical stripe near one lead of the capacitor indicates the positive lead. If the capacitor has one, large, centrally placed dot the positive lead is the right lead when the capacitor is held with the leads facing down and the dot facing you.

Install the six tantalum capacitors listed below by locating their positions on the assembly diagram or the PC board silkscreen.

(✓) C1,C3-C6 3.3 uF (Orange-Orange)
(✓) C2 33 uF (Orange-Orange)(Largest Cap)

(✓) Install the 23 ceramic decoupling capacitors where indicated on the assembly diagram or PC board silkscreen.

This completes the soldering portions of the assembly procedure. DO NOT INSTALL THE ICs AT THIS TIME.

## POWER SUPPLY TEST

With the power off insert the ROM/EROM board into the computer bus. Turn the power on, and with a voltmeter or calibrated oscilloscope measure the output of each voltage regulators at the third or highest lead (closest to the top of the board). The mounting screw of the 7805 regulator in position 3 is a convenient ground point. The regulator voltages should measure as follows:

( ) Position 1 ... 7905 ... -5V +/- .5 V
( ) Position 2 ... 7812 ... +12V +/- .5 V
( ) Position 3 ... 7805 ... +5V +/- .5 V

Do NOT continue until all voltages are correct.

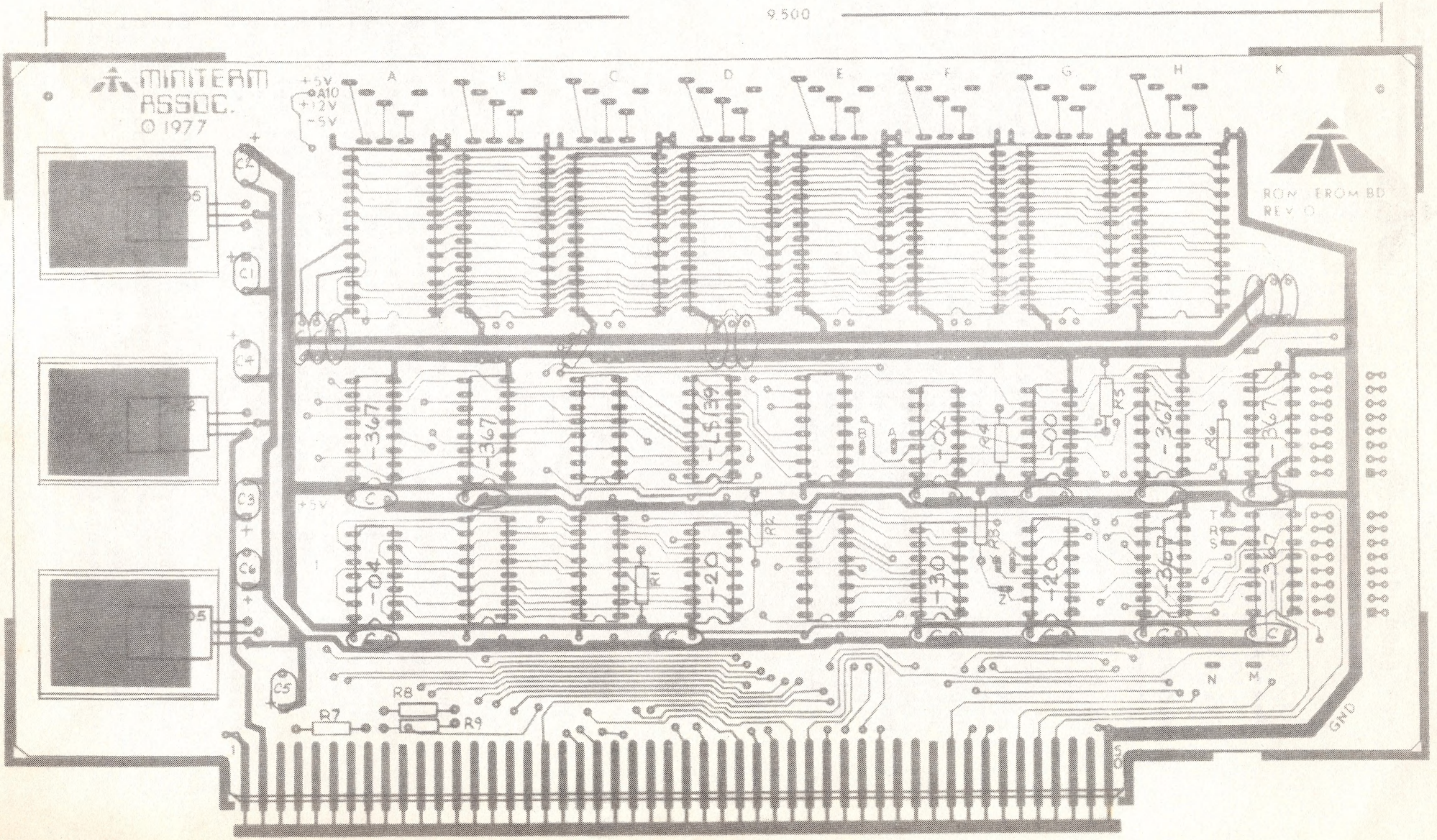
## PREPARING and INSERTING ICS

ICs come from the manufacturer with a slight outward bend of their pins away from the IC body. This aids automatic insertion equipment but makes manual insertion of the ICs into the sockets difficult. Use pliers or press the leads against a hard surface to bend the leads perpendicular.

All ICs should be inserted with the pin #1 indication (dot, notch, etc.) closest to the connector side of the board. Insert each IC according to the table below. Do NOT rely on chip labeling for pin orientation.

| | POSITION | IC TYPE |
|---|---|---|
| ( ) | A1 | 74LS04 |
| ( ) | A2 | 74LS367 |
| ( ) | B2 | 74LS367 |
| ( ) | D1 | 74LS20 |
| ( ) | D2 | 74LS139 |
| ( ) | F1 | 74LS30 |
| ( ) | F2 | 74LS02 |
| ( ) | G1 | 74LS20 |
| ( ) | G2 | 74LS00 |
| ( ) | H1 | 74LS367 |
| ( ) | H2 | 74LS367 |
| ( ) | K1 | 74LS367 |
| ( ) | K2 | 74LS367 |

ASSEMBLY DIAGRAM
**********

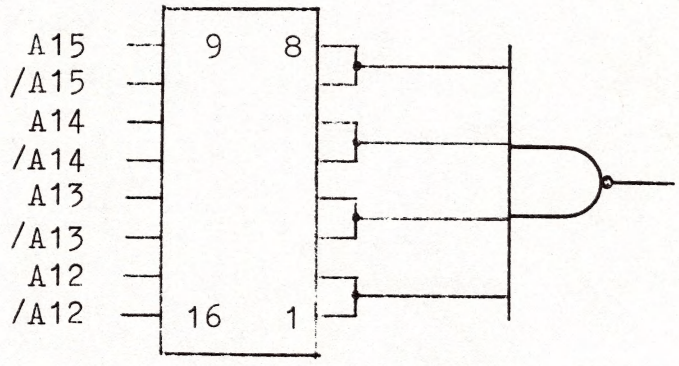


## JUMPER SELECTION

### ADDRESS SELECTION

#### 4K Block - 1K Devices

The ROM/EROM board is two separately addressable blocks of memory. Each block consists of four memory devices which may be either 1K or 2K devices. Blocks become 4K or 8K long depending on the devices used. Each block is addressed by selection of jumpers within a 16 pin DIP jumper block. The jumper block at position B1 selects the address range for memory devices at positions A3, B3, C3 and D3. The jumper block at position C1 selects the address range for memory devices at positions E3, F3, G3 and H3. Each jumper block is arranged as shown below:



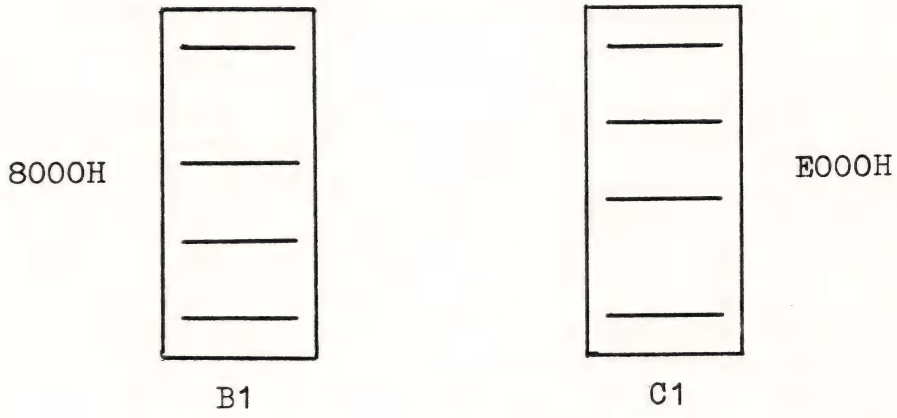

Four jumpers are used to connect either the true or inverted address data for each of the four address lines A12, A13, A14 and A15. Each combination of the four address jumpers will select 1 of 16 unique 4K address blocks. To select a particular 4K address range, express the block number (0 to 15) as a 4 bit binary number. The most significant bit represents A15 while the least significant bit represents A12. For each binary 1 connect a jumper to the true address line and for each binary 0 connect a jumper to the inverted address line.

For example, if you wanted to address the first four memory devices to the 4K address range from 8000H to 8FFFH (the 'H' indicates the number is in HEX notation) and the second four memory devices to the 4K address range E000H to EFFFH, 4 bit binary representations of 8H and EH are as shown.

8H . . . 1 0 0 0

EH . . . 1 1 1 0

With the jumpers installed the B1 and C1 jumper blocks will look like this:




The addresses assigned to each of the memory devices with this address jumper configuration are listed below:

| Device # | Position | Address Range |
|---|---|---|
| M0 | A3 | 8000H - 83FFH |
| M1 | B3 | 8400H - 87FFH |
| M2 | C3 | 8800H - 8BFFH |
| M3 | D3 | 8C00H - 8FFFH |
| M4 | E3 | E000H - E3FFH |
| M5 | F3 | E400H - E7FFH |
| M6 | G3 | E800H - EBFFH |
| M7 | H3 | EC00H - EFFFH |

NOTE: Failure to program jumper blocks B1 and C1 will cause the ROM/EROM board to be selected for all address ranges at the same time.

Also, jumper blocks B1 and C1 should not be indentically jumpered as this will cause memory devices of block #1 to conflict with those of block #2.

## ADDRESS SELECTION

### 8K Block - 2K Devices

When using either memory block for 2K devices, the block becomes 8K long. To select one of eight possible 8K address ranges, only the three most significant address bits A15, A14 and A13 are required. There are eight possible address ranges which are expressed in HEX notation below:

| 8K Block # | Address Range | Binary Block Representation |
|---|---|---|
| 0 | 0000H - 1FFFH | 000 |
| 1 | 2000H - 3FFFH | 001 |
| 2 | 4000H - 5FFFH | 010 |
| 3 | 6000H - 7FFFH | 011 |
| 4 | 8000H - 9FFFH | 100 |
| 5 | A000H - BFFFH | 101 |
| 6 | C000H - DFFFH | 110 |
| 7 | E000H - FFFFH | 111 |

Use the binary block number representation to select the address jumpers as shown in the 1K address selection section with the exception of the last address bit A12. Insert three jumpers for the three MSB address bits A15, A14, and A13 only. The A12 jumper will not be used when selecting an 8K block.

### 1K / 2K Device Selection

Jumper block C2 selects two address lines which are decoded to enable only 1 of 4 memory devices at one time. Jumper block C2 comes pre-jumpered (in foil) for the selection of 1 of 4 1K devices for both memory blocks. To use a memory block with 2K devices, jumper block C2 allows decoding address lines A11 and A12 (instead of A10 and A11) for a 1 of 4, 2K selection.

To modify the ROM/EROM board for 2K devices, carefully pry the socket body of position C2 off the socket pins. Use a thin screwdriver and pry only at the center of the socket ends to avoid prying pins loose. With a sharp tool, break the traces connecting pins 1 and 16, 3 and 14, 5 and 12, and 7 and 10. Replace the socket body. Use the table below to select 4 jumpers to program jumper block C2 for 1K or 2K operation:

1K / 2K DEVICE SELECTION TABLE

| C2 JUMPERS 1 2 3 4 5 6 7 8 / 16 15 14 13 12 11 10 9 | 1K DEVICES | 2K DEVICES |
|---|---|---|
| X X X X | M0 - M7 | - - - - |
| X X X X | - - - - | M0 - M7 |
| X X X X | M0 - M3 | M4 - M7 |
| X X X X | M4 - M7 | M0 - M43 |

"X" denotes jumper position.

BUFFER ENABLE SELECTION

Each of the eight memory devices on the ROM/EROM board may be individually enabled or disabled from the bus. The buffer enable feature allows specialty peripheral boards with small amounts of memory (or memory referenced I/O) to be addressed within the ROM/EROM address space. For example, many floppy disk interfaces such as the MiniTerm FDI have an on-board ROM bootstrap. Together with on-board RAM and memory referenced I/O, the FDI board requires 1K of address space. This small amount is sometimes difficult to fit into a system without giving up a 4 or 8K block. However, if you addressed the FDI board and one of the ROM/EROM blocks at the same address, disabling one of the EROMs gives up just 1K and also allows a restart jump to the FDI bootstrap.

E1 BUFFER ENABLE JUMPER TABLE

| Device | Position | Enable Jumper |
|---|---|---|
| M0 | A3 | 8 - 9 — enabled |
| M1 | B3 | 7 - 10 |
| M2 | C3 | 6 - 11 — enabled - RD. 6/12/83 |
| M3 | D3 | 5 - 12 |
| M4 | E3 | 4 - 13 |
| M5 | F3 | 3 - 14 |
| M6 | G3 | 2 - 15 |
| M7 | H3 | 1 - 16 |

## RESTART JUMP

### On-Board Direct Jumps

The ROM/EROM board has a built in Restart Jump feature. This feature allows the CPU to jump to any of the eight ROM/EROM memory devices directly. The jumper selects at block E2 select which ROM. The actual address to which the CPU jumps is determined by the address you have selected for that particular memory device. Note that only one 'jump address' jumper should be installed at any time. The ROM/EROM jump feature is initiated by a low on the S-100 bus PReset line pin 75. Restart will occur after a low level at pin 75. The RESET switch of S-100 computers pulls pin 75 low.

The Restart Jump feature may be disabled by removing IC G2 (74LS00).

The table below indicates the jumper to direct the restart jump to the desired memory device.

E2 RESTART-JUMP JUMPER TABLE

| MEMORY DEVICE | POSITION | JUMPER |
|---|---|---|
| M0 | A3 | 1 - 16 |
| M1 | B3 | 2 - 15 |
| M2 | C3 | 3 - 14 |
| M3 | D3 | 4 - 13 |
| M4 | E3 | 5 - 12 |
| M5 | F3 | 6 - 11 |
| M6 | G3 | 7 - 10 |
| M7 | H3 | 8 - 9 |

### Off-Board Direct Jumps

When another memory device is enabled within the selected ROM/EROM address range, as in the previous FDI example, the CPU may be directed to jump to that device by selecting the appropriate restart jumper. Select the jumper corresponding to the ROM/EROM memory device which was disabled to allow memory space for the external memory device. In the previous FDI example, the CPU would automatically execute the FDI ROM

bootstrap on restart.

### Indirect Jumps

When it is necessary to jump to an address not on a 1K or 2K boundary, or to jump to an address not within the ROM/EROM address range, a jump instruction may be programmed into an EROM and placed in one of the on-board memory positions. For example, if you wanted to jump to address 4AB6H on restart, you would program an unconditional jump instruction in the first three bytes of an EROM such as: C3 B6 4A, and jumper the ROM/EROM board to jump to that EROM. This EROM is then placed in one of the eight memory device positions on the ROM/EROM board with the restart jumper selected to jump to this device. The CPU will do a direct jump to the EROM and then indirectly jump to 4AB6H by executing the EROM jump instruction. When doing an indirect jump, the memory device with the programmed jump instruction must be enabled onto the bus with the proper enable jumper.

## FRONT PANELLESS OPERATION

### MWrite Logic

The MWrite signal functions to control the writing of data into memories from both the front panel and the CPU. The logic to generate this signal is normally found on the system front panel. When restart jump is combined with ROM Monitor/Editor intelligence, such as found on the MERLIN video interface with MBI firmware, the front panel functions of entering programs and controlling the computer can be more efficiently carried out from the keyboard. The MWrite logic has been designed into the ROM/EROM board to simulate the logic signals usually generated by a front panel to allow front panelless operation.

The MWrite logic is enabled by connecting jumper pads A and B on the ROM/EROM board. These are located between IC positions E2 and F2. The MWrite logic should not be enabled when the ROM/EROM board is used with a front panel. This would cause the front panel deposit circuitry to malfunction due to a bus fight on the MWrite bus line.

## Protect Status

Bus lines 20 and 70 used for the front panel memory protect feature on Altair computer systems have been tied to supply rails on the ROM/EROM board to enable memories when a front panel is not used. To retain the front panel memory protect feature on Altair computer systems, the traces to bus pins 20 and 70 should be cut with a sharp tool.

## Wait Logic

One wait state may be added to the ROM/EROM board by connecting a jumper between jumper pads M and N. These are located directly below IC position K1. The standard 2708 EROM has an access speed of 450 ns and will require no wait states when used with standard 2MHz processors.

## Memory Device Personality Jumpers

The memory device personality jumpers allow 2708 pin compatible mask ROMS to be used on the ROM/EROM board instead of, or along with, 2708 EROMS.

There are presently many 2708 'pin compatible' mask ROMS available from many manufactureres. Pin compatible is in quotes to emphasize that these devices are in general not directly plug-in compatible, just close. Mask ROMS do not require the many different supply voltages of the 2708 and the 2K versions require an extra address line. Each manufacturer has assigned these variables to the four non-standard pins 18, 19, 20 and 21 to suit his needs. Pin 20 has been defined on the ROM/EROM board as a low chip select as in the true 2708. The majority of 2708 'pin compatible' devices fit this definition. The other three lines 18, 19 and 21 have been arranged in a jumper array such that each memory device may be independently configured. Each of the three lines from each memory device may be jumpered to +5, -5, +12, GND and A10. The ROM/EROM board is supplied from the factory pre-jumpered for 2708 EROMS. The 2708 definition for pins 18, 19 and 21 is +5V, +12V, and -5V respectively.

To use a non-2708 '2708 pin compatible' device on the ROM/EROM board, check the part definition for pins 18, 19, 20 and 21. Pin 20 must be low true chip select.

Where the designations for 18, 19 and 21 differ from the standard 2708 pinout, the preset jumper must be cut and replaced with the correct one. Each memory device position has three vertical jumpers at the top of the board. From left to right these are pin 18, 19 and 21 respectively. The jumper busses for +5, -5, -12 and A10 have been labelled on the ROM/EROM board. The pads closest to the memory devices are ground pads.

## 2K 2716 EROMS

Both Intel and TI have introduced a 2K version of the popular 2708 EROM and called it a 2716. However, these parts are not equivalent owing to a difference in pinout. In particular, the TI part has defined pin 20 as A10 while Intel has retained the low true chip select definition of the 2708. The Intel part is compatible with the ROM/EROM board whereas the TI part will require board modification to swap the A10 and CE inputs.

## Bank Select

The ROM/EROM board has provisions for extending the computer address space to 128K. Memory expansion is accomplished by controlling the state of bus line 60 with a memory control board (not available from MiniTerm) or I/O port. A 128K system will consist of two 64K memory banks. One bank will be enabled when a high logic level is present on bus line 60 and the other bank will be enabled when a low logic level is present. To use this ROM/EROM feature, add a jumper between pads Y and Z to enable the board on a high logic level, or between pads X and Z to enable the board on a low logic level.

## THEORY OF OPERATION

### Memory Array

The ROM/EROM board contains eight positions (M0 - M7) for 2708 compatible memory devices. The memory devices are connected in a parallel array. Only the individual chip selects are separately controlled. The chip selects enable the output buffers of one of the eight memory devices to drive the ROM/EROM internal data bus. The internal data bus is buffered by tri-state drivers (H2, K2) to drive the S-100 Data In bus. The bus drivers are controlled by the Buffer Enable logic. All address lines driving the memory array are buffered by tri-state drivers A2 and B2. Pins 18, 19 and 21 of each memory position are initially tied to supply lines for 2708 operation. However, each position may be individually jumpered to suit non-2708 ICs.

### Address Selection

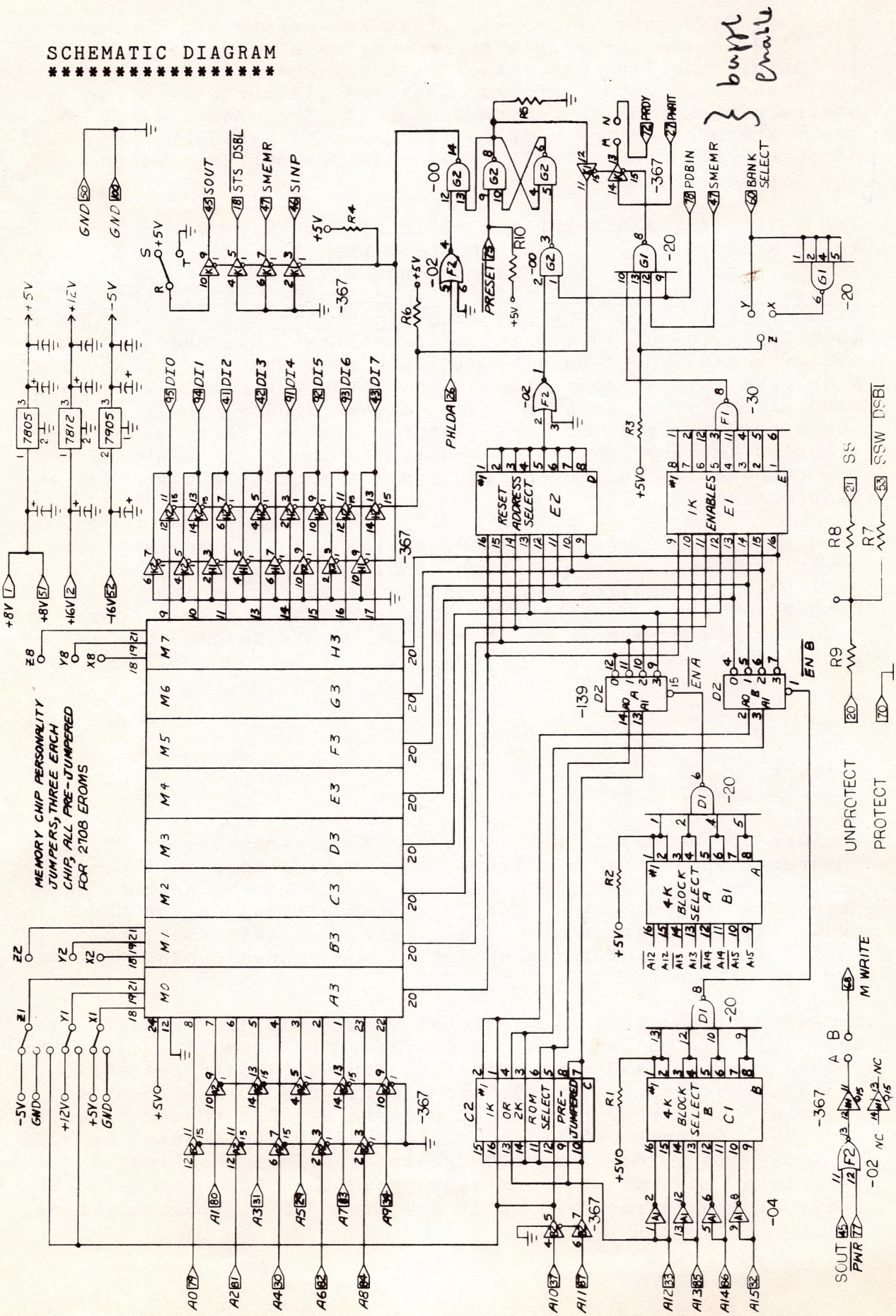
Each of two blocks of four memory devices on the ROM/EROM may be individually addressed in memory. Address selection is accomplished by providing both the true address and the inverted address for selection in a DIP jumper block. Address lines A12 through A15 are inverted by the four A1 inverters and applied to DIP jumper blocks B1 and C1. The four input NAND gates of IC D1 detect all ones when the selected address is present and provide low enables to the dual 1-of-4 decoders of D2. The low on the D2 enable pin allows D2 to decode the two address inputs A10 and A11 and provide a low true chip select to one of the memory device positions. For more information on Address Selection see the Address Jumper section of this manual.

### Buffer Enables

The chip selects from the decoder D2 enable one memory device to output data onto the ROM/EROM internal data bus. Data does not reach the S-100 bus (and consequently the CPU) unless the tri-state output drivers H2 and K2 have been enabled. During normal memory operation (not restart jump),

# SCHEMATIC DIAGRAM

**********



pin 8 of NAND gate G2 is low. This low propagates through the k1-11,12 buffer to enable the memory data onto the S-100 Data In bus by enabling the output data drivers H2, K2. This low will not propagate through the k1-11,12 buffer unless the enable pin which is connected to pin 8 of NAND gate G1 is low. Therefore, any low on the input to NAND gate G1 will disable the data output drivers and the ROM/EROM board will not appear in memory.

The S-100 signals SMEMR and PDBIN will be high to indicate a valid memory read condition from the CPU. Pin 13 of NAND gate G1 is tied high by resistor R3. This input may be pulled low by a true or false condition on the Bank Select line depending on whether jumper pad X or Y is used. When this line is pulled low it indicates that this memory bank is not selected and should be disabled from the bus. Pin 10 of NAND gate G1 is connected to the output of the eight input NAND gate F1. Each of the eight inputs to F1 may be connected to one of the memory device chip selects. A selected memory device will pull its input to NAND gate F1 low through a buffer enable jumper and cause a high on the NAND output.

Whenever the selected memory device has its buffer enable jumper missing, an all high condition on the inputs of F1 will prevail causing a low on the F1 output which disables NAND gate G1 and in turn the ROM/EROM data output buffers. In this way each memory device may be individually enabled or disabled in memory.

## Restart Jump

Because of the way in which the RO/EROM board does its "jump", "Restart Jump" is a misnomer and could more correctly be called "restart NOP to address". The ROM/EROM board "executes a jump" by forcing NOP instructions on the CPU data bus. Recall that a NOP is all zeros and that the only CPU action during a NOP execution is the incrementing of the program counter.

A restart condition is detected when the S-100 PReset line (pin 75) is pulled low. A low on pin 75 sets the cross-coupled NAND gate flip flop formed by G2-8 and G2-6 to restart condition. This forces pin 8 of G2 high which disables the ROM/EROM output drivers H2, K2 through buffer K1. The restart condition at pin 8 of G2 in inverted by NAND gate G2-11. The inverted restart signal enables the K1 tri-state control bus drivers and the H1, K2 data bus drivers. The buffer K1-5 pulls low the /Status Disable line.

This causes the CPU status bus to tri-state including the memory and I/O control signals SMEMR, SOUT, and SINP. The remaining three enabled tri-state drivers of K1 control these signals to disable all system memory and I/O devices from the data bus. For as long as the inverted restart signal is low, the only device driving the S-100 Data In bus will be the ROM/EROM drivers H1, K2. The drivers have their inputs tied low to form the NOP instruction op-code. After the PReset line is pulled low to initiate the restart operation, the CPU has reset its program counter to address zero. As it processes the forced NOP instructions the CPU program address counter is incremented. This contiues until the address is incremented into the ROM/EROM address space. The ROM/EROM decodes the CPU program address until it decodes the memory position for which a Jumper has been placed in the Reset Address Select Jumper Block. The decoded signal is inverted in F2-1 and gated with PDBIN in NAND gate G2-3. A coincidence of the decoded signal with PDBIN puts a low on the reset input of the cross-coupled NAND gate flip flop G2-8,6. The flip flop resets and bus control returns to the CPU which is at the desired ROM/EROM address. The decoded signal is gated by PDBIN to avoid resetting the flip flop on decoding glitches which occur at address transition time.

The restart operation may be interrupted by a Direct Memory Access (DMA) to memory. The PHLDA (Hold Acknowledge) S-100 Signal at pin 26 is sampled to determine if a DMA state exists. When PHLDA is high indicating a DMA state, F2-4 applies a low disable signal to pin 12 of NAND gate G2-11. This disables the tri-state control and data buffers and allows the DMA device to access system memory.

## SPECIAL CASES

### TDL ZPU Board

The TDL ZPU board is not fully S-100 compatible. S-100 CPU boards have the status bus and control bus separately controllabled by the /Status Disable signal (pin 18), and the /Control Disable signal (pin 19) respectively. These lines exist only as the /Status Disable signal on the TDL ZPU board. The effect of this design is to mask the CPU control signals (PDBIN, PWR, etc.) whenever the status bus is tri-stated. The ROM/EROM board tri-states the status bus to perform the restart jump.

The ROM/EROM board may be used to restart jump the ZPU board by reinserting IC K1 such that its pin 5 and pin 9 are outside the IC socket. This is a brute force approach to controlling the SMEMR status line and the same one TDL uses to restart its ZPU from the TDL system monitor board.